

CLAIMS

1. A delay locked loop apparatus comprising:
 - a first delay element to receive a reference signal, to delay the reference signal by a
 - 5 delay time, and to output a first delayed signal;
 - a second delay element to receive the first delayed signal, to delay the first signal
 - delayed signal by the delay time, and to output a second delayed signal; and
 - a harmonic lock prevention circuit to receive the reference signal, the first delayed
 - signal, and the second delayed signal, and to adjust the delay time so that a period of each
 - 10 delayed signal is within a predetermined range.
2. The apparatus of claim 1 wherein the harmonic lock prevention circuit further comprises:
 - 15 a first current steering phase detector to receive the reference signal and the first
 - delayed signal and to output a signal based on a state of the first delayed signal;
 - a second current steering phase detector to receive the reference signal and the second
 - delayed signal and to output a signal based on a state of the second delayed signal; and
 - a delay time adjustment circuit to increase the delay time if the state of the first
 - 20 delayed signal is high, to decrease the delay time if the state of the second delayed signal is
 - low, and to output a harmonic lock prevent signal if the state of the first signal is low and the
 - state of the second signal is high.
- 25 3. The apparatus of claim 1 wherein the delay locked loop further comprises a residual
- phase error correction circuit to receive the harmonic lock prevented signal and to correct a
- residual phase error in the delayed signals.

4. The apparatus of claim 1 wherein a boundary of the predetermined range is less than an integer multiple of a period of the reference signal.
- 5 5. The apparatus of claim 1 wherein the predetermined range of the period of each delayed signal has a first boundary that is greater than one-half the period of the reference signal and a second boundary that is less than three-halves the period of the reference signal.
- 10 6. The apparatus of claim 1 wherein the first delay element further comprises six transistors.
- 15 7. The apparatus of claim 2 wherein the a first current steering phase detector comprises an NMOS tree of XNOR gates.